RESEARCH DEPARTMENT

Experimental equipment for converting television signals into digital signals and vice versa

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RESEARCH DEPARTMENT

EXPERIMENTAL EQUIPMENT FOR CONVERTING TELEVISION SIGNALS INTO DIGITAL SIGNALS AND VICE VERSA

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SUMMARY

The report describes equipment which has been constructed for converting a television signal into digital form and reconverting to conventional form. The television signal is sampled at a rate of 13 x 10^6 samples/sec and a 6-bit digital signal is derived which indicates the magnitude of each sample as one of 64 binary numbers. It was found that good-quality colour and monochrome pictures are obtained from a 6-bit digital system with many types of subject matter, but at least 7, and possibly 8, bits would be required to ensure that a digital system never caused perceptible defects.

1. INTRODUCTION

The fundamental aspects of applying digital techniques to television have already been described in a previous report.[1] This report describes equipment which has been constructed to convert a 625-line video signal having a bandwidth of 5·5 MHz into a digital signal and vice versa. The equipment operates at a rate of 13 x 10^6 samples per second and converts the magnitude of each sample into a 6-bit binary number.

Many types of analogue-to-digital converter have been developed but the particular combination of speed and resolution demanded by television signals makes the choice far from obvious. Converters using counting or successive approximation and involving some form of feedback network are easily capable of providing sufficient resolution but cannot at present be used at the speeds required for television signals. An open loop system is therefore necessary and this may be either a parallel or serial system, or a combination of both.

In the basic form of parallel converter, the video signal is fed to a large number of level-comparators connected in parallel, there being one level-comparator and a suitable reference voltage for each quantum level in the quantized signal. This type of converter is capable of the high speeds needed for television but requires a large number of electronic components.

In the serial or propagation type of converter, the first stage determines the state of the most significant bit, the second stage determines the state of the second most significant bit and so on. The total number of stages in such a converter is therefore equal to the number of bits required per sample. This means that the serial type of converter requires fewer components than the parallel type but problems arise due to the difficulty of avoiding the introduction of spurious switching signals. Difficulties also arise in the design of the very stable, wide-band circuits required to handle the partly analogue and partly digital signals occurring in this type of converter.

Successful converters for television based on both the serial[2] and parallel[3] systems have been constructed but the form of analogue-to-digital converter we have developed employs a combination of both systems in an attempt to minimise their individual disadvantages.

Digital-to-analogue conversion is far simpler than analogue-to-digital conversion and conventional techniques are used for this process.

For convenience, the analogue-to-digital converter will be referred to as the 'a.d.c.' and the digital-to-analogue converter will be referred to as the 'd.a.c.'

2. ANALOGUE-TO-DIGITAL CONVERTER

2.1. General Description

The a.d.c. provides six bits per sample but it is thought feasible to increase this to seven or possibly eight bits. These bits represent a binary number corresponding to the magnitude of each sample of the video signal.

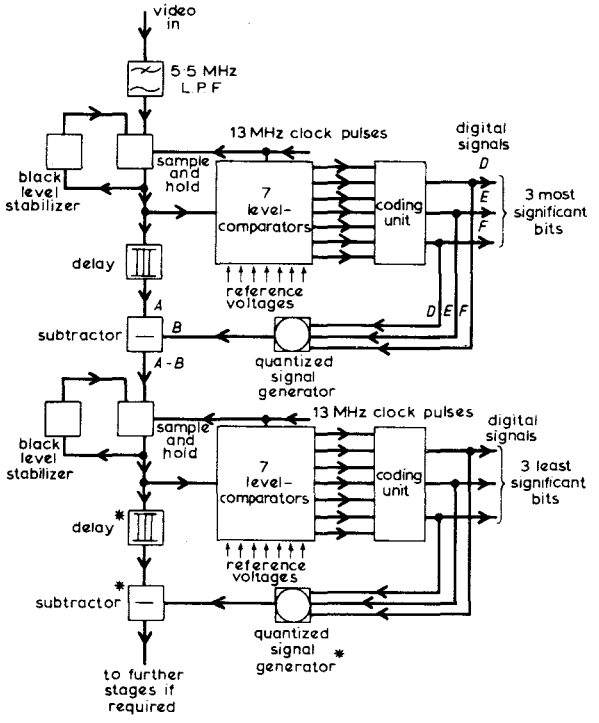

Fig. 1 - Block diagram of hybrid a.d.c.

As shown in Fig. 1, the a.d.c. has two similar sections connected in series, each section being a 3-bit parallel converter. The first section determines the states of the 3 most significant bits and the second section determines the states of the 3 least significant bits. Further lower-order bits could be determined by adding further sections, the maximum number of bits being limited by the accuracy which can be attained in practice.

In the first section of the a.d.c., seven level-comparators connected in parallel are fed with a video signal which has been sampled and held at the 13 MHz clock pulse rate, and has its black level accurately stabilised to a fixed potential. The outputs of these seven level-comparators change state when the video signal crosses the voltage levels $(V/8)$ x 1, 2, 3, 4, 5, 6 and 7 where V is the peak voltage of the video signal with respect to black level. (It is assumed in this section that the video signal does not contain any information below black level. The coding of synchronizing pulses is discussed in Section 2.2.).

The coding unit converts the outputs from the level-comparators into three digital signals indicating the states of the three most significant digits of a binary number representing the magnitude of the video signal. The digital signals, D, E and F obtained during the typical black-to-white transition shown in Fig. 2(a) are shown in Figs. 2(d), (e) and (f). The binary numbers corresponding to different ranges of video level are indicated on the right-hand side of Fig. 2(a).

In order to obtain further lower-order bits, it is first necessary to decode the three most significant bits to give an 8-level video signal in which the voltage difference between successive levels is exactly $V/8$ (see Fig. 2(b)). By subtracting this signal from the original video signal, a signal is obtained which indicates the amount by which the video signal is greater than the highest reference voltage it has exceeded (see Fig. 2(c)). (The delay inserted in the video path between the sample and hold unit and the subtractor (see Fig. 1) is necessary to compensate for the delay in the quantized signal path.)

The second section of the a.d.c. is identical to the first except that the reference voltages fed to the level-comparators are one eighth of those fed to the first section. This section divides the difference signal obtained from the first section

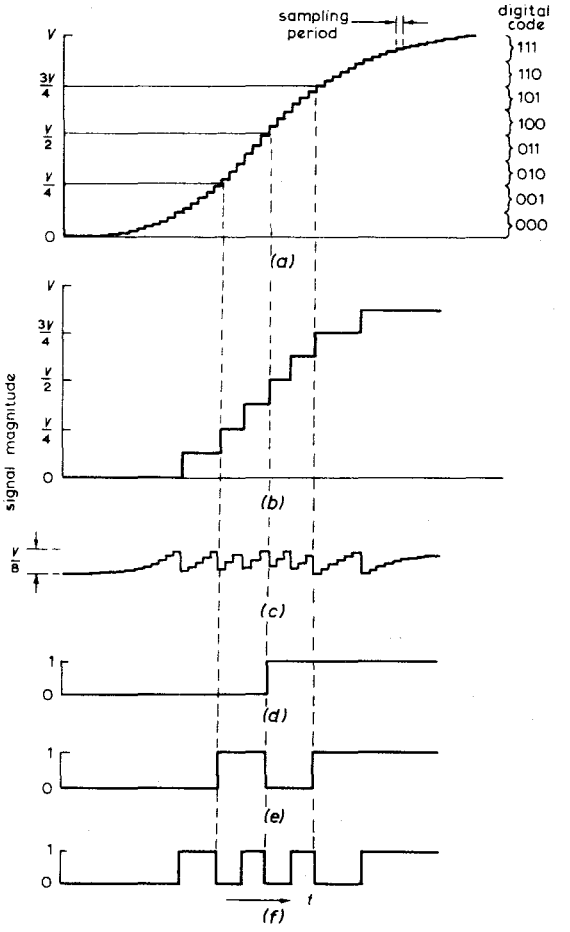

Fig. 2 - Typical waveforms in first section of a.d.c.

(*a*) Sampled and held video signal (A in Fig. 1)
(*b*) Quantized video signal (B in Fig. 1)
(*c*) Output of first section ($A-B$ in Fig. 1)
(*d*) Most significant digit (D in Fig. 1)
(*e*) Second most significant digit (E in Fig. 1)
(*f*) Third most significant digit (F in Fig. 1)

into a further 8 parts with the result that the original video signal is divided into 64 parts by the two sections combined. The digital outputs of the second section indicate the fourth, fifth and sixth most significant bits in each sample. The purpose of the sample and hold unit at the beginning of the second section is to remove switching 'spikes' which are generated when a change in quantum levels occurs in the first section. This is shown in Fig. 3. The sampling pulses are timed so as to avoid coincidence with any switching 'spikes' which may be present.

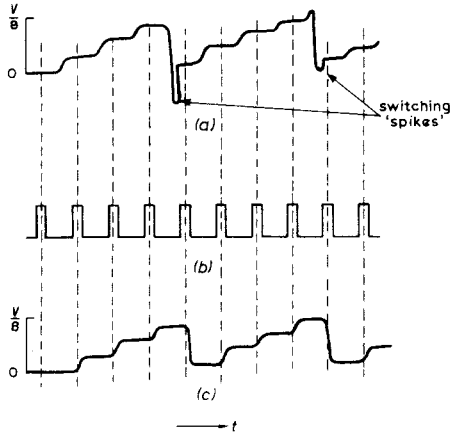

Fig. 3 - Waveforms illustrating removal of switching spikes by second sample and hold circuit

(*a*) Input to sample and hold unit (*b*) Sampling pulses
(*c*) Output of sample and hold unit

The six digits corresponding to one sample are brought into coincidence by means of delays inserted in the digital outputs of the first stage. All digital outputs are finally sampled by clock pulses so that a digital '1' is indicated by the presence of a pulse and a digital '0' by the absence of a pulse.

The units marked '*' in Fig. 1 are not required for a 6-bit converter but are needed if it is desired to obtain further lower-order bits.

2.2. Transmission of Sync Pulses

In the description of the analogue-to-digital converter given above, only video information between black and white levels has been converted and therefore no synchronizing information is present in the digital signals.

The simplest method of including synchronizing pulses is to encode the composite video signal between the tips of sync pulses and white level. Using this system with a normal monochrome signal, 30% of the available quantum levels are used for the synchronizing pulses. This is wasteful of transmission capacity as it is possible to accurately convey the synchronizing information by a much smaller percentage of the available levels. The simple method is not so wasteful, however, with colour signals in which the colour sub-carrier signals may also extend below black level.

In order to obtain the minimum possible wastage of transmission capacity, a system was devised in which the black level was adjusted to occur one quantum level above the lowest level. The presence of a synchronizing pulse was then detected by all digital outputs being simultaneously in their '0' state. A disadvantage of this system is that the exact timing of a particular synchronizing pulse is not conveyed with sufficient accuracy and it is therefore necessary to insert a flywheel sync-pulse regenerator in the signal path at the output of the d.a.c.

Some of the units in the a.d.c. will now be discussed in more detail.

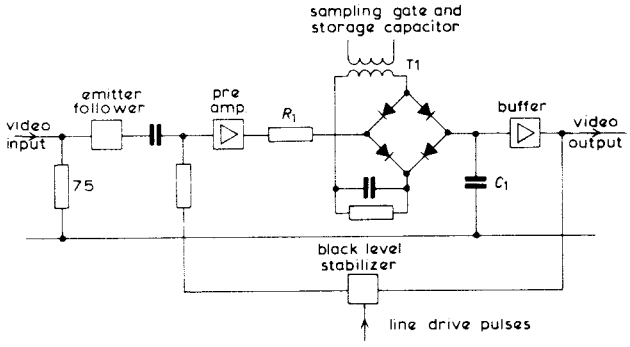

Fig. 4 - Sample and hold unit

2.3. Sample and Hold Unit

The basic sample and hold circuit consists of a four-diode gate and storage capacitor C_1 as shown in Fig. 4. The interval between sampling pulses is about 80 ns and C_1 is connected to the source of video signal by these pulses for about 35 ns. The holding time is therefore about 45 ns. A photograph illustrating the performance of this circuit is shown in Fig. 5.

The pre-amplifier connecting the signal source to the four-diode gate gives an output signal with a peak-to-peak amplitude of about 5 volts. Also it has a small output impedance to permit fast charging of C_1. The purpose of the resistance R_1 is to critically damp the charging action. Without this resistance, the voltage held on C_1 overshoots its correct value due to stray inductance in the charging circuit.

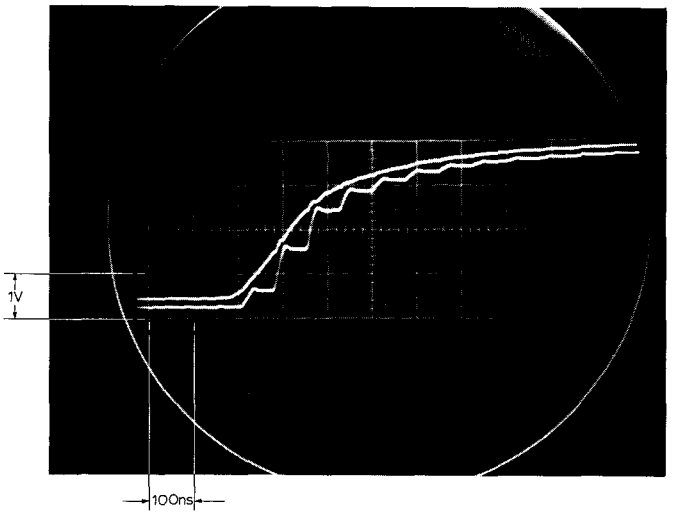

Fig. 5 - Video input (upper waveform) and output (lower waveform) of sample and hold unit

The buffer stage following C_1 has a sufficiently high input impedance to prevent any appreciable leakage during the holding interval. This stage has unity gain over the frequency band from 0 to about 50 MHz and its output is connected directly to the level-comparators.

The black level of the video signal at the output of the buffer stage is held at 0 volt by a conventional black-level stabilizing circuit.

A somewhat similar form of sample and hold unit is described in more detail in Reference 4.

2.4. Level-Comparators

Each of these units is required to provide an output signal with two stable states depending on whether the video signal level is above or below the given reference level. Any error between the actual and intended voltage levels at which the change of state occurs must be small compared with the difference in voltage between adjacent quantum levels. Since the video signal fed to the level-comparators has a black-to-white magnitude of 5 volts and it is to be divided into 64 quantum levels, errors in the change-over level must be considerably less than 80 mV. Further requirements of the comparator are that the rise-time of the output signal should be short compared with the interval between sampling pulses, and the delay through the entire unit should be as brief as possible. In practice, the rise-time is about 10 ns and the delay is about 40 ns.

A block diagram of a level-comparator unit is shown in Fig. 6. The video signal is fed to one input of a high-gain differential amplifier, the other input being connected to a reference voltage. A voltage difference of more than 2·5 mV between the two inputs is sufficient to establish the output voltage at its 'high' or 'low' limiting state. The purposes of the sampling and bistable units shown in Fig. 6 are to ensure that the output of the comparator does not change state in the middle of a sampling period and that its voltage level has only two stable states. In the pulse train from the sampling unit, 'high' and 'low' outputs from the differential amplifier are indicated by positive and negative clock pulses respectively. These pulses trigger the tunnel-diode bistable circuit. The clock pulses fed to the sampling unit are delayed by about 40 ns with respect to those fed to the sample and hold unit in order to allow for delays in the differential amplifier and in the video path.

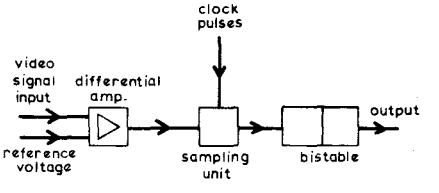

Fig. 6 - Level-comparator unit

2.5. Quantized Signal Generator and Subtractor

In practice the quantized signal generator and subtractor units are combined in a single unit, a diagram of which is shown in Fig. 7. The quantized signal (see Fig. 2(*b*)) is derived by adding binary-weighted versions of the three digital signals from the coding unit (see Fig. 2(*d*), (*e*) and (*f*)). These weighted digital signals are obtained from the switches S1, S2 and S3 in Fig. 7, S1 being operated by the most significant bit, S2 by the second most significant bit and S3 by the third most significant bit. The three weighted digital signals are then added at the input to the amplifier giving an eight-level quantized video signal. By arranging that the quantized signal is of opposite polarity to the video input signal the required difference signal appears at the output of the amplifier (see Fig. 2(*c*)).

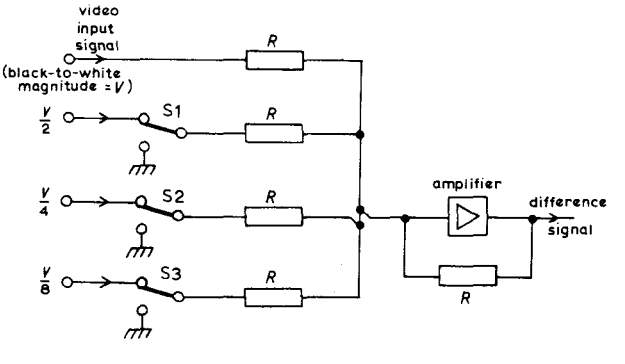

Fig. 7 - Quantized signal generator and subtractor

3. DIGITAL-TO-ANALOGUE CONVERTER

3.1. General Description

The d.a.c. was designed to convert the digital signals from the a.d.c. back into an analogue video signal. The digital signals are supplied to the d.a.c. by six separate wires, each handling a separate bit. Other possible forms of d.a.c. are described in Reference 5.

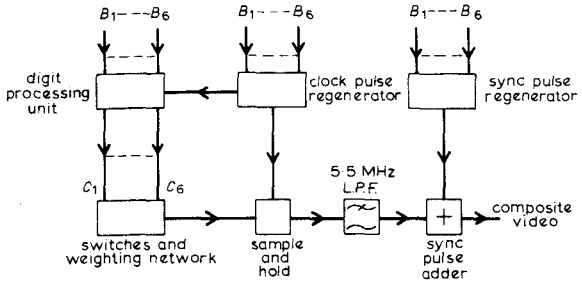

Fig. 8 - Block diagram of digital-to-analogue converter

$B_1 \ldots B_6$ represent digital inputs to the d.a.c.

A block diagram of the d.a.c. is shown in Fig. 8. The principle of its operation is that the digital signals, after suitable processing, control switches which allow binary-weighted currents to flow through a common resistance as shown in Fig. 9. Pulses representing the most significant bit control a current with a weighting of ½, those representing the second most significant bit control a current with a weighting of ¼ and so on. The signal thus developed across the common resistance is a quantized version of the video signal applied to the original converter.

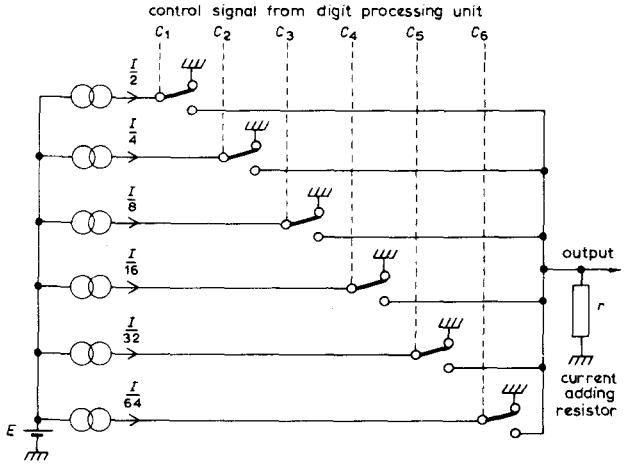

Fig. 9 - Switches and weighting network

In order to remove switching spikes from this quantized signal, each sample is re-sampled by clock pulses after transient disturbances associated with switching have had time to decay. Clock pulses are regenerated in the decoder by adding the incoming digital signals and applying the resulting signal to a tuned amplifier resonating at the clock pulse frequency of 13 MHz.

Unwanted frequency components in the quantized signal resulting from the 13 MHz sampling process are removed by a low-pass filter with a cut-off frequency of 5·5 MHz. The synchronizing-pulse regenerator is used if the sync pulses are coded by the economical method described in Section 2.2.

The main parts of the d.a.c. will now be described in more detail.

3.2. Digit Processing Unit

This unit provides separate control signals for each bit, these being used to switch currents on or off in the weighting network in response to '1' or '0' digital input signals. The control signal remains in its '1' state until a digital '0' is received, and vice versa, thus ensuring that the number of switching transitions is kept to a minimum. All control waveforms are made to switch simultaneously by only allowing switching to occur in the presence of a clock pulse.

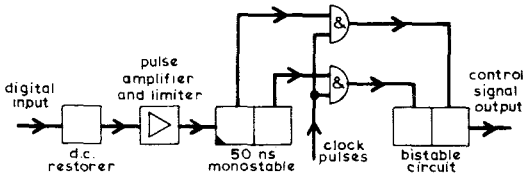

Fig. 10 - Digit processing unit

A block diagram showing the method of deriving one of the control signals from its digital input is shown in Fig. 10; the waveforms and relative timings of signals in this unit are shown in Fig. 11. After d.c. restoration, which sets the '0' state at a given d.c. potential, the digital signal is amplified and limited to produce fixed amplitude pulses whose width is then increased to 50 ns by means of a monostable circuit. The two outputs of this monostable

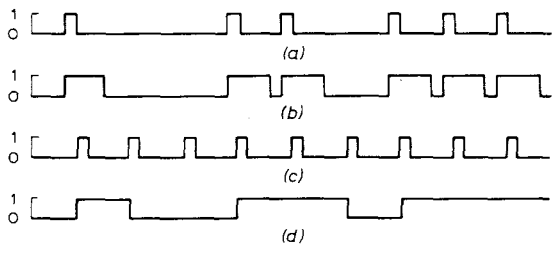

Fig. 11 - Waveforms in digit processing unit

(a) Digital input signal
(b) Output of 50 ns monostable circuit
(c) Clock pulses
(d) Control signal

circuit, which are opposite in polarity to one another, are fed to two AND gates to which clock pulses are also applied. In this way, two pulse trains are obtained, one of which contains clock pulses during the digital '1's, while the other contains clock pulses during digital '0's. These two pulse trains set and re-set a bistable circuit, the output of which provides the required control signal.

3.3. Weighting Network

A diagram of the type of weighting network used in the decoder is shown in Fig. 9.

The control signal C_1 is derived from the most significant bit, C_2 is derived from the second most significant bit and so on. These control signals operate switches in such a manner that a constant-current generator is connected to the common resistance r when a '1' occurs in the appropriate control signal. By summing the binary-weighted currents in the resistance r, a voltage is obtained which is an analogue equivalent of the digital input signal.

The value chosen for the resistance r was 75 ohms. This value was selected as a compromise between several requirements. It should be low to achieve fast response times; on the other hand, it should be high enough to give an output voltage which is large in comparison with spurious switching signals. In order to achieve a large output voltage, the magnitude of the current from the constant current generators should also be as large as possible. These currents are limited mainly by the maximum power dissipation which could be allowed without causing any undesirable drifting in component value due to increase in temperature. The value of the current corresponding to the most significant bit, which was finally selected, was 6·5 mA, giving a maximum output voltage of about 1 volt.

The practical circuit arrangement of one current-weighting path and its associated switch is shown in Fig. 12. The resistance R controls the magnitude of the current and the transistor TR1 gives the current source a high output impedance. By making the control signal positive or negative with respect to the voltage across the resistance r, the current from TR1 is routed through D1 or D2 respectively.

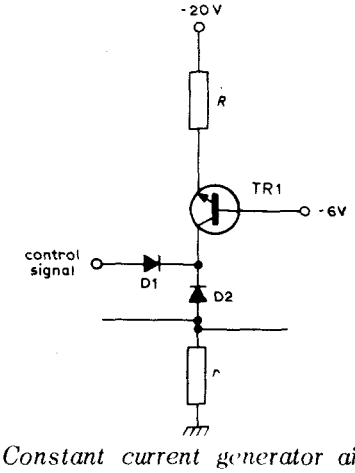

Fig. 12 - Constant current generator and switch in weighting network

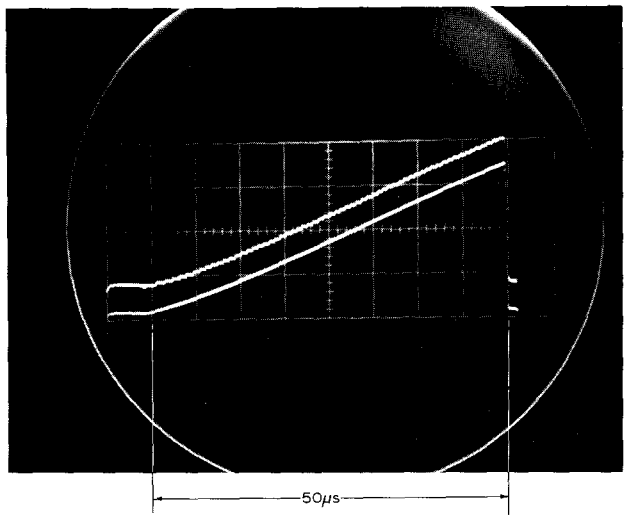

Fig. 13 - Overall performance of a.d.c. and d.a.c. to line sawtooth input signal

4. PERFORMANCE

The overall performance of the a.d.c. and d.a.c. for slowly changing video signals is illustrated in Fig. 13. This figure shows the quantized video signal obtained from the d.a.c. (top waveform) using a 6-bit system when a line sawtooth video signal is applied to the a.d.c. (bottom waveform). It can be seen that the quantum levels are substantially equally spaced over the whole grey-scale, indicating that the required accuracy for a 6-bit digital television system has been obtained.

The performance of the system for rapidly changing input signals may be judged to a certain extent by the fact that coding and decoding of composite colour signals including a 4·3 MHz colour sub-carrier caused very little degradation in the final display on a colour monitor beyond that to be expected by quantizing into a fixed number of brightness levels.

The effect of coding and decoding monochrome signals using varying numbers of bits per sample is illustrated in Fig. 14. It can be seen that with this particular picture, quantization causes easily visible contouring effects in plain areas when 4 bits or less are used, but it is extremely difficult to detect any degradation of the picture with 6 bits per sample. With some types of subject matter, however, the effects of quantization using 6 bits per sample are obvious; in particular, large areas in which the brightness varies slowly from one edge to the other show noticeable striations.

(*a*)

(*b*)

(*c*)

(*d*)

(*e*)

(*f*)

Fig. 14 - Effect of number of bits in the digital system on a television display

(*a*) 2 brightness levels (1 bit)
(*b*) 4 brightness levels (2 bits)
(*c*) 8 brightness levels (3 bits)
(*d*) 16 brightness levels (4 bits)
(*e*) 32 brightness levels (5 bits)
(*f*) 64 brightness levels (6 bits)

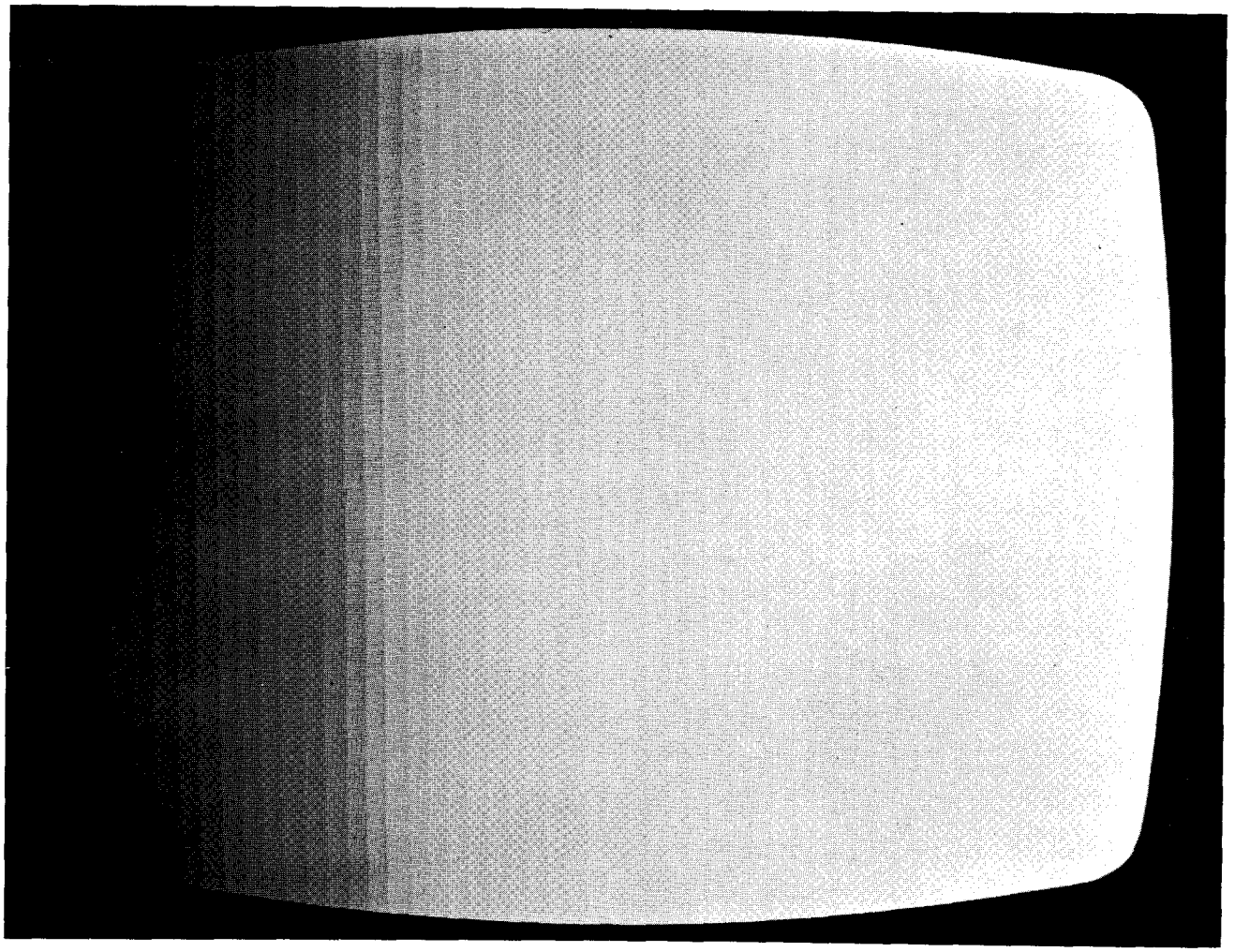

Fig. 15 - Display of line sawtooth waveform with 64 brightness levels (6 bits)

This point is illustrated in Fig. 15 which shows the display obtained from a line sawtooth waveform (see Fig. 13) using 6 bits per sample. While the effects of using a 6-bit system are not normally as visible as those shown in Fig. 15, this figure indicates that at least 7 bits (128 levels) and possibly 8 bits (256 levels) would be required by a digital television system offering broadcast quality.

5. CONCLUSIONS

The successful construction of a 6-bit a.d.c. and d.a.c. for television signals has proved the feasibility of these components for digital television equipment. For practical use 7 or 8 bits would be needed but designs of a.d.c. and d.a.c. which have been developed could be extended without difficulty. It is therefore possible to evolve digital television equipment as soon as suitable storage and arithmetic units are made available.

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